IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Atty. Docket No.:

001701.00236

Koji SAKUI et al.

Serial No.:

Continuation of 10/202,886, filed July

Group Art Unit:

Unknown

Filed:

26, 2002 Herewith

Examiner:

Unknown

For:

NONVOLATILE SEMICONDUCTOR

MEMORY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with Applicants' duty of disclosure, the following information is submitted for consideration by the United States Patent and Trademark Office in connection with the above-captioned application. The information is identified on the attached PTO-1449 form.

This application relies, under 35 U.S.C. § 120, on the earliest filing date of prior U.S. patent application serial nos. 10/202,886, filed July 26, 2002; 09/921,570, filed August 6, 2001; and 09/393,201, filed September 9, 1999. The documents identified on the attached PTO 1449 form were submitted to and/or cited by the Office in a prior application and, therefore, copies are not required to be provided in this application. (See 37 C.F.R. § 1.98(d)).

Applicants do not waive any right to take appropriate action to establish patentability over the listed documents should they be applied as references against the claims of the present application.

It is respectfully requested that the Examiner fully consider each of the documents, initial the enclosed Form PTO-1449 in the appropriate place to indicate that the document has been

considered, and return a copy of the initialed form to the undersigned in accordance with MPEP Section 609.

Applicants believe that no fee is necessary pursuant to 37 C.F.R. § 1.97(b). However, if a fee is due, the Office is authorized to charge Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: August 12, 2003

By:

Gary D. Fedorochko

Registration No. 35,509

1001 G Street, N.W. Washington, D.C. 20001-4597 (202) 508-9100

GDF:lab

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PTO/SB/08A (08-00)
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Substitute for form 1449A/PTO **INFORMATION DISCLOSURE** STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet of 2

Complete if Known				
Application Number	TBA			
Filing Date	Herewith			
First Named Inventor	Koji Sakui et al.			
Group Art Unit	Unknown			
Examiner Name	Unknown.			
Attorney Docket Number	01701.00236			

				U.S. PATENT DOCU	MENTS	14
Examiner Initials *	Cite No.1	U.S. Patent Document Numbe		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
				Neukomm	01-13-1987	
		5,043,942	B1	lwata et al.	08-27-1991	
		5,379,254	B1	Chang	01-1995	
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FOREIGN PATENT DOCUMENTS									
Examiner Initials*	Foreign Patent Document		Cite	Name of Patentee	Date of Publication of	Pages, Columns, Lines, Where Relevant			
	No.1	Office ³	Number⁴		Code ⁵ nown)	or Applicant of Cited Document	Cited Document MM-DD-YYYY	Passages or Relevant Figures Appear	T ₆
		EP	044026	65	Α		08-07-1991	•	
		EP	07048	52	A2		04-03-1996		
	:	JP	11-1957	'18			07-21-1999		abst
		JP	2-2328	98	Α	NCE Corp	09-14-1990		abst

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Substitute	e for form 1449A/PTC)			Complete if Known
				Application Number	TBA
INFC	RMATION	DIS	CLOSURE	Filing Date	Herewith
STATEMENT BY APPLICANT				First Named Inventor	Koji Sakui et al.
				Group Art Unit	Unknown
	(use as many she	ets as	necessary)	Examiner Name	Unknown.
Sheet	2	of	2	Attorney Docket Number	01701.00236

		OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS	
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"SESSION XII: ROMs, PROMs AND EROMs THPM 12.6:A 16Kb Electrically Erasable Nonvolatile Memory", William S. Johnson, et al. ISSCC 80/1980, IEEE International - Solid-State Circuits Conference, CH 1490-2/80/0000/0152, pp. 152-153, Feb. 14, 1980	
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		"New Ultra High Density EDPROM And Flash EEPROM With NAND Structure Cell", Fujio Masuoka, et al., CH2515-5/87/0000-0552 1987 IEEE, IEDM 87 pp. 552-555, May 1987	
	,	Chapter 1 Basics of Nonvolatile Semiconductor Memory Devices, p. 70; Chapter 4 Floating Gate Flash Memories, p. 212; Chapter 5 SONOS Nonvolatile Semiconductor Memories, p. 316; p. 326, 5.1 The SONOS Nonvolatile Memory Transistor, p. 327: Chapter 5 SONOS Nonvolatile Semiconductor Memories, p. 344, (Undated)	
		European Search Report dated September 22, 2000	
,		Art Lancaster et al., ISSCC Dig. Tech. Papers, "Nonvolatile Memory," February 1983, pp. 164-165	
		Yoshiaki Kamigaki et al., IEEE J. of Solid-State Circuits, Vol. 24, No. 6, "Yield and Reliability of MNOS EEPROM Products," December 1989, pp. 1714-1722	
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Examiner	Date
Signature	Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.